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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/721,879	11/26/2003	Harold Theodore Devor	P-6216-US	6009

49444 7590 08/08/2006

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EXAMINER	
FENNEMA, ROBERT E	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/721,879	DEVOR ET AL.	
	Examiner	Art Unit	
	Robert E. Fennema	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *5/25/2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-28 are pending. Claims 1, 9, 17, 21 have been amended as per applicants request.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-7, 9-15, 21-26 and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Hohensee et al. (USPN 6,064,815, herein Hohensee).

4. As per Claim 1, Hohensee teaches: A method comprising:

During translation of a code block from a first format suitable for a first computing platform to a second format suitable for a second computing platform (Column 1, Lines 45-47 and Column 1, Line 62-Column 2, Line 4), detecting misaligned data access resulting from execution of said code block (Column 3, Lines 4-9 shows the detector detecting an exceptional condition, and Column 2, Lines 61-67 show the exception to be caused by a misaligned memory reference); and

modifying said code block according to said misaligned data access (Column 8, Lines 58-66, additional code is added to the instruction stream to handle the

misalignment).

5. As per Claim 2, Hohensee teaches: The method of claim 1, wherein detecting comprises performing instrumentation of said code block to detect whether execution of said code block results in the misaligned data access (Column 3, Lines 4-9. The exceptional condition detector is an instrument (as defined by The Dictionary of Computers, Information Processing & Telecommunications, where instrumentation is taken to mean "what is required to measure a complex activity, such as the performance level of a computer system, whether hardware or software", where a detector measures the misaligned data access in this case), and does the detecting of the misalignment).

6. As per Claim 3, Hohensee teaches: The method of claim 2, wherein detecting comprises performing instrumentation of at least one instruction in said code block to detect a location of an instruction whose execution results in the misaligned data access (Column 3, Lines 15-17. In order to substitute code for an instruction, the location would necessarily have to have been detected).

7. As per Claim 4, Hohensee teaches: The method of claim 1, wherein detecting comprises performing instrumentation of at least one instruction in said code block to detect a location of an instruction whose execution results in the misaligned data access (Column 3, Lines 15-17. In order to substitute code for an instruction, the location would

necessarily have to have been detected).

8. As per Claim 5, Hohensee teaches: The method of claim 1, wherein modifying comprises adding to said code block an instruction to branch an execution of said code block to a code sequence whose execution handles the misaligned data access (Column 12, Lines 23-30. A branch to a Fixup code block is called to handle the misalignment).

9. As per Claim 6, Hohensee teaches: The method of claim 1, wherein modifying comprises modifying said code block to handle misaligned data access in a subsequent execution of said code block (Column 12, Lines 23-30. A branch to a Fixup code block is called to handle the misalignment).

10. As per Claim 7, Hohensee teaches: The method of claim 1, further comprising translating said code block from said first format to said second format (Column 1, Line 62 – Column 2, Line 4).

11. As per Claim 9, Hohensee teaches: An apparatus comprising:

a processor to detect, during translation of a code block from a first format suitable for a first computing platform to a second format suitable for a second computing platform (Column 1, Lines 45-47 and Column 1, Line 62-Column 2, Line 4) misaligned data access resulting from execution (Column 3, Lines 4-9 shows the

detector detecting an exceptional condition, and Column 2, Lines 61-67 show the exception to be caused by a misaligned memory reference), of said code block, and

to modify said code block according to said misaligned data access (Column 8, Lines 58-66, additional code is added to the instruction stream to handle the misalignment).

12. As per Claim 10, Hohensee teaches: The apparatus of claim 9, wherein the processor is able to perform instrumentation of said code block to detect whether execution of said code block results in the misaligned data access (Column 3, Lines 4-9. The exceptional condition detector is an instrument, and does the detecting of the misalignment).

13. As per Claim 11, Hohensee teaches: The apparatus of claim 10, wherein the processor is able to perform instrumentation of at least one instruction in said code block to detect a location of an instruction whose execution results in the misaligned data access (Column 3, Lines 15-17. In order to substitute code for an instruction, the location would necessarily have to have been detected).

14. As per Claim 12, Hohensee teaches: The apparatus of claim 9, wherein the processor is able to perform instrumentation of at least one instruction in said code block to detect a location of an instruction whose execution results in the misaligned data access (Column 3, Lines 15-17. In order to substitute code for an instruction, the

location would necessarily have to have been detected).

15. As per Claim 13, Hohensee teaches: The apparatus of claim 9, wherein the processor is able to add to said code block an instruction to branch an execution of said code block to a code sequence whose execution handles the misaligned data access (Column 12, Lines 23-30. A branch to a Fixup code block is called to handle the misalignment).

16. As per Claim 14, Hohensee teaches: The apparatus of claim 9, wherein the processor is able to modify said code block to handle misaligned data access in a subsequent execution of said code block (Column 12, Lines 23-30. A branch to a Fixup code block is called to handle the misalignment).

17. As per Claim 15, Hohensee teaches: The apparatus of claim 9, wherein the processor is able to, before detecting the misaligned data access, translate said code block from said first format to said second format (Column 1, Line 62 – Column 2, Line 4).

18. As per Claim 21, Hohensee teaches: A machine-readable medium having stored thereon a set of instructions that, if executed by a machine, cause the machine to perform a method comprising:

during translation of a code block from a first format suitable for a first computing platform to a second format suitable for a second computing platform (Column 1, Lines 45-47 and Column 1, Line 62-Column 2, Line 4) detecting misaligned data access resulting from execution of said code block (Column 3, Lines 4-9 shows the detector detecting an exceptional condition, and Column 2, Lines 61-67 show the exception to be caused by a misaligned memory reference); and

modifying said code block according to said misaligned data access (Column 8, Lines 58-66, additional code is added to the instruction stream to handle the misalignment).

19. As per Claim 22, Hohensee teaches: The machine-readable medium of claim 21, wherein the instructions that result in detecting result in performing instrumentation of said code block to detect whether execution of said code block results in the misaligned data access (Column 3, Lines 4-9. The exceptional condition detector is an instrument, and does the detecting of the misalignment).

20. As per Claim 23, Hohensee teaches: The machine-readable medium of claim 22, wherein the instructions that result in detecting result in performing instrumentation of at least one instruction in said code block to detect a location of an instruction whose execution results in the misaligned data access (Column 3, Lines 15-17. In order to substitute code for an instruction, the location would necessarily have to have been

detected).

21. As per Claim 24, Hohensee teaches: The machine-readable medium of claim 21, wherein the instructions that result in detecting result in performing instrumentation of at least one instruction in said code block to detect a location of an instruction whose execution results in the misaligned data access (Column 3, Lines 15-17. In order to substitute code for an instruction, the location would necessarily have to have been detected).

22. As per Claim 25, Hohensee teaches: The machine-readable medium of claim 21, wherein the instructions comprise at least part of a translator (Column 1, Lines 45-48 disclose a translator).

23. As per Claim 26, Hohensee teaches: The machine-readable medium of claim 21, wherein the instructions comprise at least part of an execution layer (The instructions run throughout Hohensee's invention are executed, which necessitate them being in the execution layer).

24. As per Claim 28, Hohensee teaches: The machine-readable medium of claim 21, wherein the instructions comprise at least part of a compiler (Column 1, Lines 45-48, where a translator is a compiler).

Claim Rejections - 35 USC § 103

25. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. Claims 8 and 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hohensee.

27. As per Claim 8, Hohensee teaches the method of claim 1, but fails to teach: wherein detecting comprises detecting a misaligned data access resulting from an execution of a code block translated from a format suitable for a 32-bit based computing platform to a format suitable for a 64-bit based computing platform. Hohensee teaches that a host processor, in an execution environment, may emulate operations performed by an emulated microprocessor, but not the sizes of the processor and the emulated processor. The Examiner is taking official notice that it is well known in the art that most computer processors operate on a number of bits that are a power of 2, for example, 8, 16, 32, 64, and 128, and that a primary difference between computer processors (of the same or similar instruction set) are a difference in the bit-size of the processors. *In re Rose*, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955) teaches that it is within the skill of one of ordinary skill in the art to change size, so whether the emulation required was from 8 to 16 bits, 16 to 32 bits, or 32 to 64 bits is irrelevant to one of ordinary skill in

the art. Therefore, one of ordinary skill in the art would have been able to make use of Hohensees invention, and apply it to a 64-bit processor running a 32-bit program.

28. As per Claim 16, Hohensee teaches the apparatus of claim 9, but fails to teach: wherein the first computing platform is a 32-bit based computing platform and the second computer architecture is a 64-bit based computing platform. Hohensee teaches that a host processor, in an execution environment, may emulate operations performed by an emulated microprocessor, but not the sizes of the processor and the emulated processor. The Examiner is taking official notice that it is well known in the art that most computer processors operate on a number of bits that are a power of 2, for example, 8, 16, 32, 64, and 128, and that a primary difference between computer processors (of the same or similar instruction set) are a difference in the bit-size of the processors. *In re Rose*, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955) teaches that it is within the skill of one of ordinary skill in the art to change size, so whether the emulation required was from 8 to 16 bits, 16 to 32 bits, or 32 to 64 bits is irrelevant to one of ordinary skill in the art. Therefore, one of ordinary skill in the art would have been able to make use of Hohensee's invention, and apply it to a 64-bit processor running a 32-bit program.

29. As per Claim 17, Hohensee teaches: A computing platform comprising:

a processor to detect, during translation of a code block from a first format suitable for a first computing platform to a second format suitable for a second computing platform (Column 1, Lines 45-47 and Column 1, Line 62-Column 2, Line 4)

misaligned data access resulting from execution (Column 3, Lines 4-9 shows the detector detecting an exceptional condition, and Column 2, Lines 61-67 show the exception to be caused by a misaligned memory reference) of said code block, and

to modify said code block according to said misaligned data access (Column 8, Lines 58-66, additional code is added to the instruction stream to handle the misalignment); and

a dynamic random access memory operably associated with said processor to store at least a portion of said code block (Figure 1 discloses a memory, but Hohensee does not explicitly teach the memory being a dynamic random access memory (herein DRAM). However, the Examiner is taking official notice that using a DRAM for computer memory is well known in the art, due to its cheap cost and widespread use, which would have motivated one of ordinary skill in the art to utilize a DRAM in Hohensee's invention).

30. As per Claim 18, Hohensee teaches: The apparatus of claim 17, wherein the processor is able to perform instrumentation of said code block to detect whether execution of said code block results in the misaligned data access (Column 3, Lines 4-9. The exceptional condition detector is an instrument, and does the detecting of the misalignment).

31. As per Claim 19, Hohensee teaches: The apparatus of claim 18, wherein the processor is able to perform instrumentation of at least one instruction in said code

block to detect a location of an instruction whose execution results in the misaligned data access (Column 3, Lines 15-17. In order to substitute code for an instruction, the location would necessarily have to have been detected).

32. As per Claim 20, Hohensee teaches: The apparatus of claim 17, wherein the processor is able to perform instrumentation of at least one instruction in said code block to detect a location of an instruction whose execution results in the misaligned data access (Column 3, Lines 15-17. In order to substitute code for an instruction, the location would necessarily have to have been detected).

33. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hohensee, in view of Drongowski.

34. As per Claim 27, Hohensee teaches: The machine-readable medium of claim 21, wherein the instructions comprise at least part of an operating system. While Hohensee does not explicitly disclose an operating system, it would have been very obvious to one of ordinary skill in the art to be able to make use of misalignment correction capabilities on the operating-system level, so that all programs and programmers can make use of it, as well as the fact that operating systems are extremely common on most computing systems. Drongowski teaches an example of an operating system (The Alpha Linux) that makes use of commands to fix alignment problems (Section 2.7), and explains the problems misalignment can cause. Therefore, it would have been obvious to one of

ordinary skill in the art at the time the invention was made to allow an operating system to run these instructions and make use of Hohensee's invention.

Response to Arguments

35. Applicant's arguments filed 5/25/2006 have been fully considered but they are not persuasive. Applicant has argued that Hohensee describes a system wherein an original program is translated into a translated program, and is then executed and handled, and does not teach detecting the misaligned data during the translation phase. However, the Applicants claim language states that the detection of the misaligned address results from execution of the code block. Examiner directs Applicant to Column 1, Line 61 – Column 2, Line 4, which discloses that the translation process is performed for all or part of the program when the processor begins to process the program, and that instructions or groups of instructions (code blocks) may be translated as the processing proceeds, thus the translation occurs at the same time as the code is executed.

36. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., detecting a misaligned data access during the translation of a code block, and not while executing, as Applicant has argued Hohensee teaches) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988

F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The Applicant has claimed that during translation, the misaligned data access is detected resulting from execution of a code block, which means that the instruction must have been executed or been in the process of being executed to be detected, which is taught by Hohensee as explained above.

Conclusion

37. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert E. Fennema whose telephone number is (571) 272-2748. The examiner can normally be reached on Monday-Friday, 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Robert E Fennema
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